LISTING OF CLAIMS

1. (Currently Amended) A stream routing unit for routing each of a plurality of input packet streams to any of a plurality of destinations, the stream routing unit comprising:

a plurality of input ports for receiving respective input streams;

a plurality of output ports associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at addressable locations each identifiable by an address;

an assignment data structure identifying for each input stream at least one destination to which each input packet stream is to be routed; and

a packet allocation data structure holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held, the packet allocation data structure further holding information identifying the output ports associated with the intended destinations ~~destination~~ of a held ~~the~~ packet, the information being derived from the assignment data structure.

2. (Original) The stream routing unit according to claim 1, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports.

3. (Previously Presented) The stream routing unit according to claim 1, wherein the assignment data structure is a data matrix.

4. (Original) The stream routing unit according to claim 1, wherein the packet allocation data structure is an array of slots, each slot holding a source identifier and associated address.

5. (Original) The stream routing unit according to claim 4, wherein the packet allocation data structure is associated with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet.

6. (Currently Amended) The stream routing unit according to claim 4, wherein information identifying the output ports associated with the intended destination of the held packet is provided by a set of destination pointers, each destination pointer associated with a respective output port and each destination pointer being configured to point to a slot in the array which holds a source identifier and address of a packet intended for a particular destination associated with a particular output port.

7. (Original) The stream routing unit according to claim 1, wherein the packets of a said input stream are of a common length.

8. (Currently Amended) A data communication system for routing incoming packets to at least one destination, the system comprising:

a plurality of packet stream sources each generating a packet stream;

a stream routing unit comprising:

a plurality of input ports for receiving respective input packet streams;

a plurality of output ports associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at addressable locations each identifiable by an address;

an assignment data structure identifying for each input stream at least one destination to which each input packet stream is to be routed; and

a packet allocation data structure holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held, the packet allocation data structure further holding information identifying the output ports associated with the intended destinations ~~destination~~ of a held ~~the~~ packet, the information being derived from the assignment data structure; and

a plurality of destinations for receiving packets of the packet streams generated by the sources.

9. (Original) The data communication system according to claim 8, wherein at least one of the destinations comprises a programmable transport interface.

10. (Original) The data communication system according to claim 8, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports.

11. (Currently Amended) A method of routing packet streams from a plurality of sources to any of a plurality of destinations, the method comprising:

receiving said packet streams;

identifying for each input packet stream at least one destination to which each input packet stream is to be routed using an assignment data structure;

holding each packet of the packet stream in a storage means at an addressable location identifiable by an address in that [[a]] storage means;

holding for each new incoming packet a packet allocation data structure which stores a source identifier identifying the origin of the packet and the address in the storage means where the packet is held;

holding information in an assignment data structure identifying the intended destination of the packet derived from the assignment data structure; ~~and~~

using said assignment data structure information identifying the intended destination to further include in the packet allocation data structure information identifying output ports associated with intended destinations of a held packet;

routing ~~route~~ the packet from the storage means to the or each output port associated with the respective identified destination(s).

12. (Original) The method according to claim 11, wherein the input packet streams have a lower bit rate than output streams into which they are merged at the output ports.

13. (Currently Amended) The method according to claim 11, wherein said information identifying the output ports associated with the intended destination of the held packet is provided by a set of destination pointers, said method further comprising:

associating each destination pointer with a respective output port; and

configuring each destination pointer to point to a source identifier and address of a packet intended for the destination associated with that output port.

14. (Original) The method according to claim 11 further comprising:

holding each new incoming packet in a packet allocation data structure having a plurality of slots;

holding in each slot a source identifier and associated address; and

associating each slot with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet.

15. (Currently Amended) A device for delivering incoming packets to at least one destination, the device comprising:

an addressable memory which stores incoming packets at a plurality of address locations in the memory;

a source to destination matrix for mapping at least one source to at least one destination;

a packet allocation table for associating a source and at least one destination for a particular packet with the address location in the addressable [[a]] memory where ~~location at which~~ the particular packet is stored; and

an algorithm for controlling removal of the incoming packets from a memory to at least one destination, wherein the incoming packets have a lower bit-rate than packets delivered to the at least one destination.

16. (Original) The device of claim 15 further comprising a memory for holding the incoming packets at addressable locations each identifiable by an address.

17. (Original) The device of claim 15 further comprising:

a plurality of input ports for receiving respective input packets; and

a plurality of output ports associated with respective destinations to which the input packets can be routed.

18. (Currently Amended) A method for delivering incoming packets to at least one destination, the method comprising:

storing incoming packets at a plurality of addressable locations in memory;

mapping at least one source to at least one destination;

associating a source and at least one destination for a particular packet with the address location in [[a]] memory where ~~location at which~~ the particular packet is stored; and

controlling removal of the incoming packets from a memory to at least one destination, wherein the incoming packets have a lower bit-rate than packets delivered to the at least one destination.

19. (Original) The method of claim 18 further comprising holding the incoming packets at addressable locations each identifiable by an address.

20. (Original) The method of claim 18 further comprising:

receiving respective input packets; and

routing outgoing packets through a plurality of output ports associated with respective destinations.

21. (Original) The method of claim 18, wherein mapping further comprises creating a source to destination matrix.

22. (Original) The method of claim 18, wherein the at least one destination is a programmable transport interface.

23. (Original) The method of claim 18, wherein the memory is an SRAM memory.

Claims 24-31. (Canceled).

32. (New) The stream routing unit according to claim 6, wherein the destination pointers are assigned by an algorithm.

33. (New) The stream routing unit according to claim 32, wherein after the assignment of destination pointers is completed, the algorithm controls the storage means to output a packet according to the status of the destination pointers.

34. (New) The stream routing unit according to claim 1, wherein held packets are output in the order in which they are received.

35. (New) The stream routing unit according to claim 1, further comprising means for outputting the held packet only when all of the output ports associated with the intended destinations of the held packet are free.

36. (New) A stream routing unit, comprising:

a plurality of input ports, each input port receiving an input packet stream;

a plurality of output ports, each output port outputting an output packet stream;

a memory including a plurality of addressable memory locations;

a source-to-destination matrix storing data identifying, for each source of the input packet streams coupled to the input ports, one or more destinations, for packets within those input packet streams, which are coupled to receive the output packet streams from the output ports;

a processor for storing packets of the input packet streams in the memory and for retrieving stored packets from the memory to form the output packet streams;

the processor filling a packet allocation table which includes a plurality of slot locations, each slot location storing a source identifier which identifies a source of the received packet stream to which a given packet belongs linked in the packet allocation table to an address in the memory for the addressable memory location where that given packet has been stored by the processor;

a destination pointer, associated with each one of the output ports, implemented by the processor for pointing to a slot location in the packet allocation table from which the address of the given packet is retrieved, the destination pointer pointing to the slot location in accordance with the destination data stored in the source-to-destination matrix;

the processor retrieving the given packet from the memory at the address provided in the slot location pointed at by the destination pointer, sending the retrieved given packet to each output port associated with the destination that is linked in the source-to-destination matrix with the source identified in the slot location for inclusion in the output packet stream of the output port.

37. (New) The stream routing unit of claim 36 further comprising a write pointer implemented by the processing means for pointing to an open slot location in the packet allocation table to which the source identifier and address of the given packet are written.

38. (New) The stream routing unit of claim 36, wherein a bit rate of the input packet streams is lower than a bit rate of the output packet streams.